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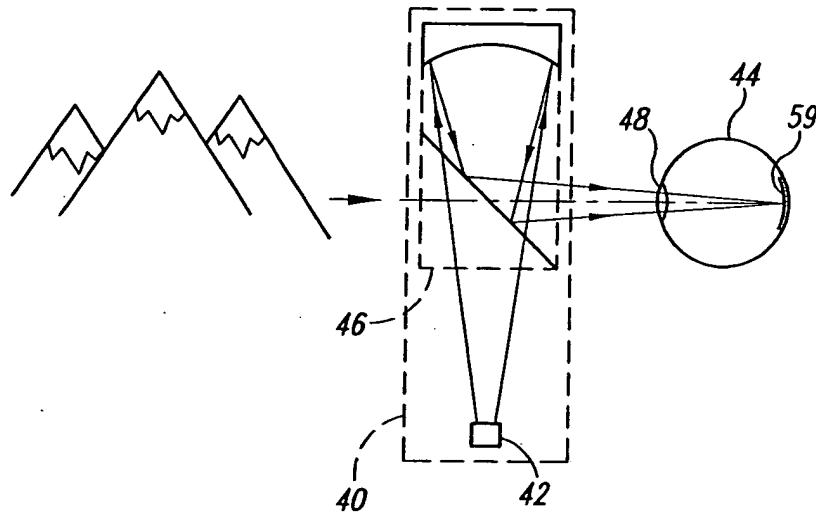


Fig. 1

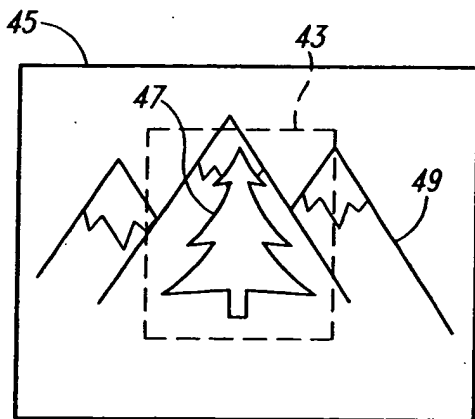


Fig. 2A

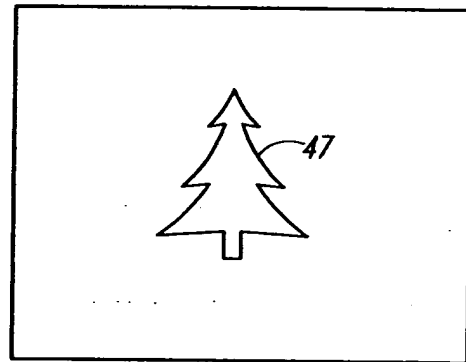
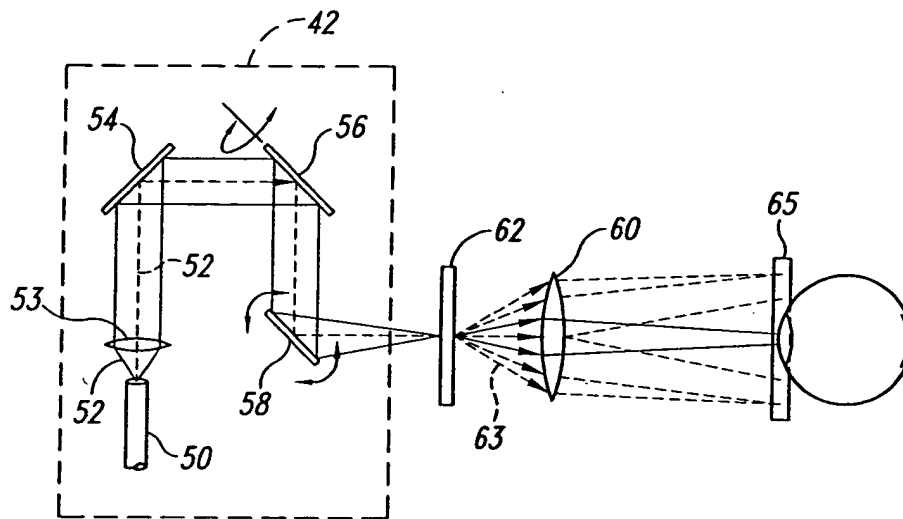
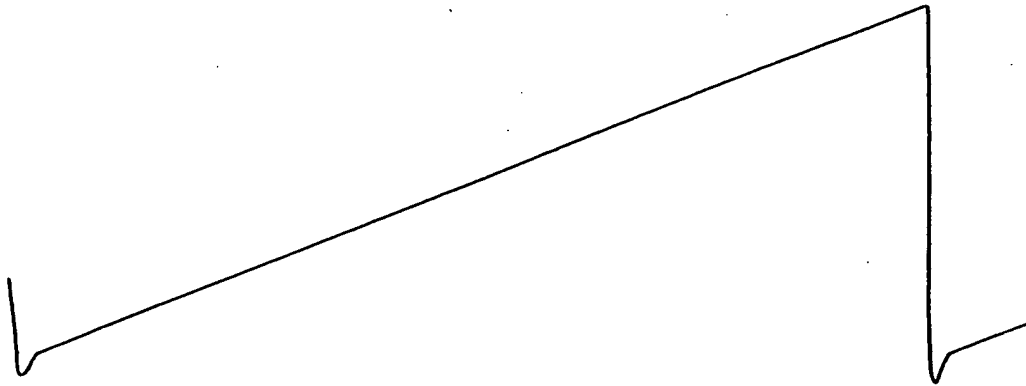


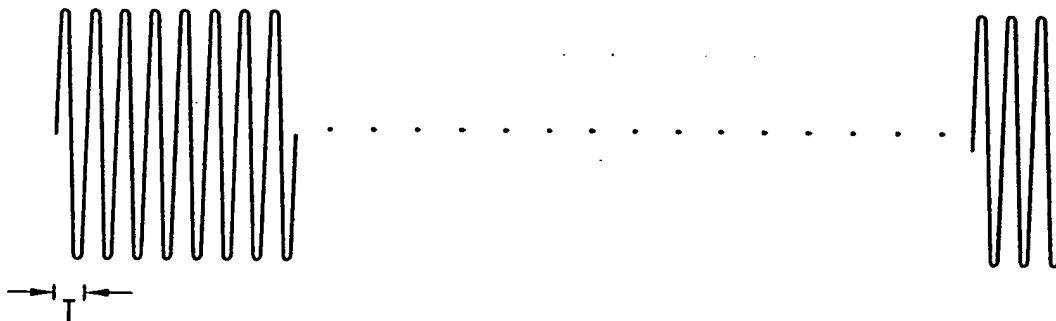
Fig. 2B



*Fig. 3*



*Fig. 4A*



*Fig. 4B*

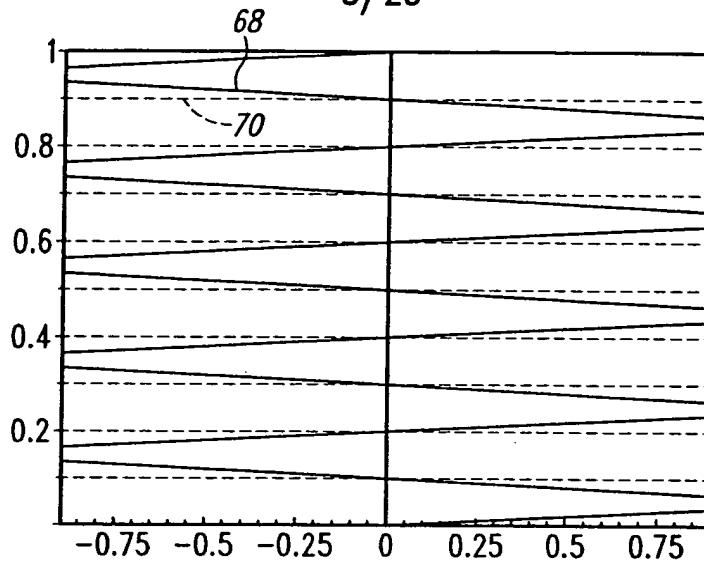


Fig. 5

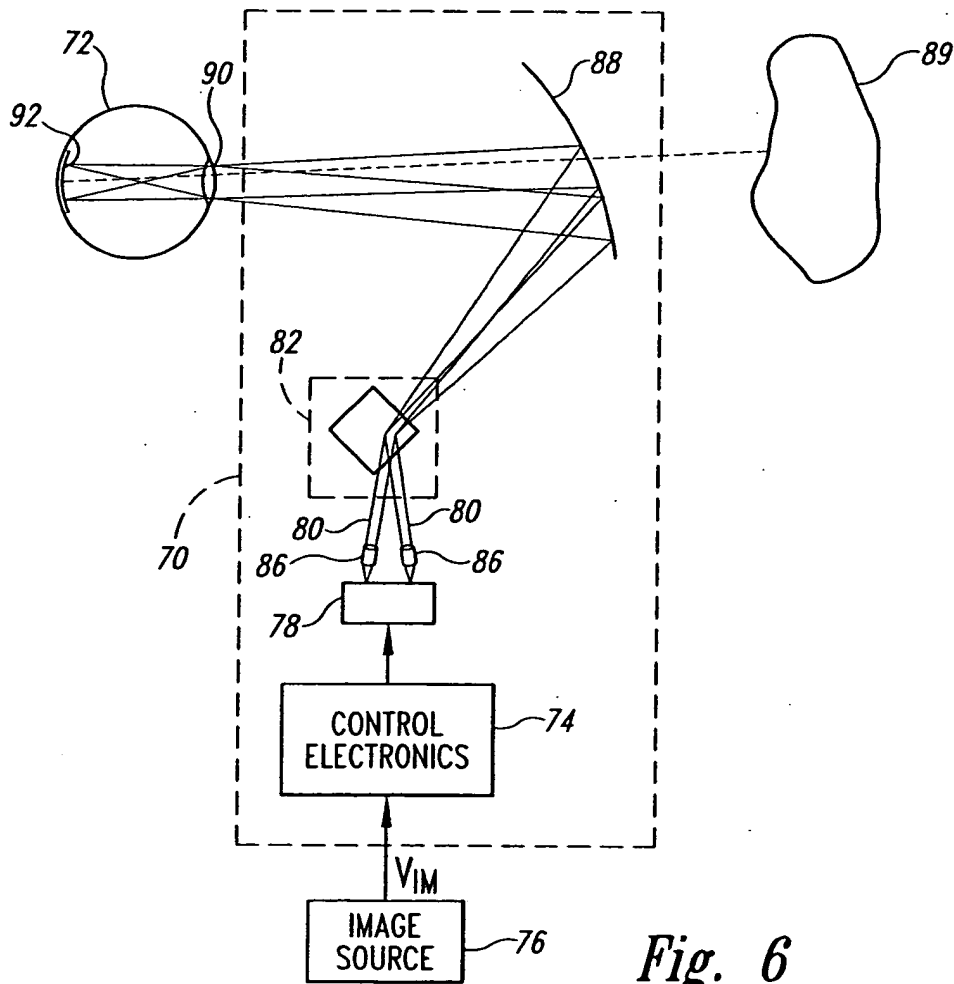
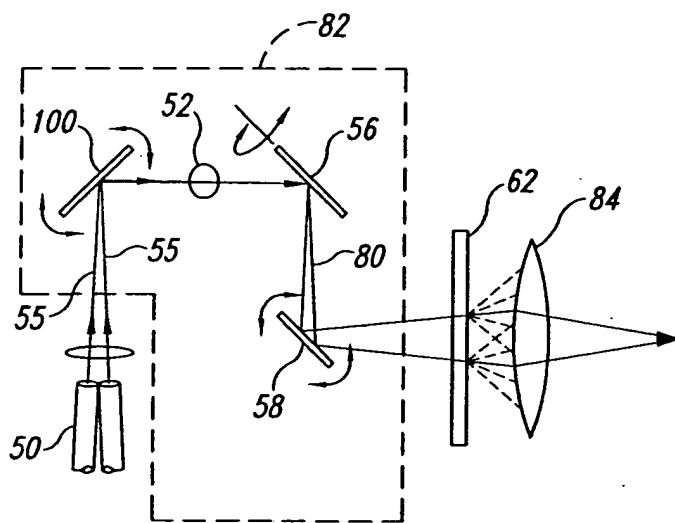
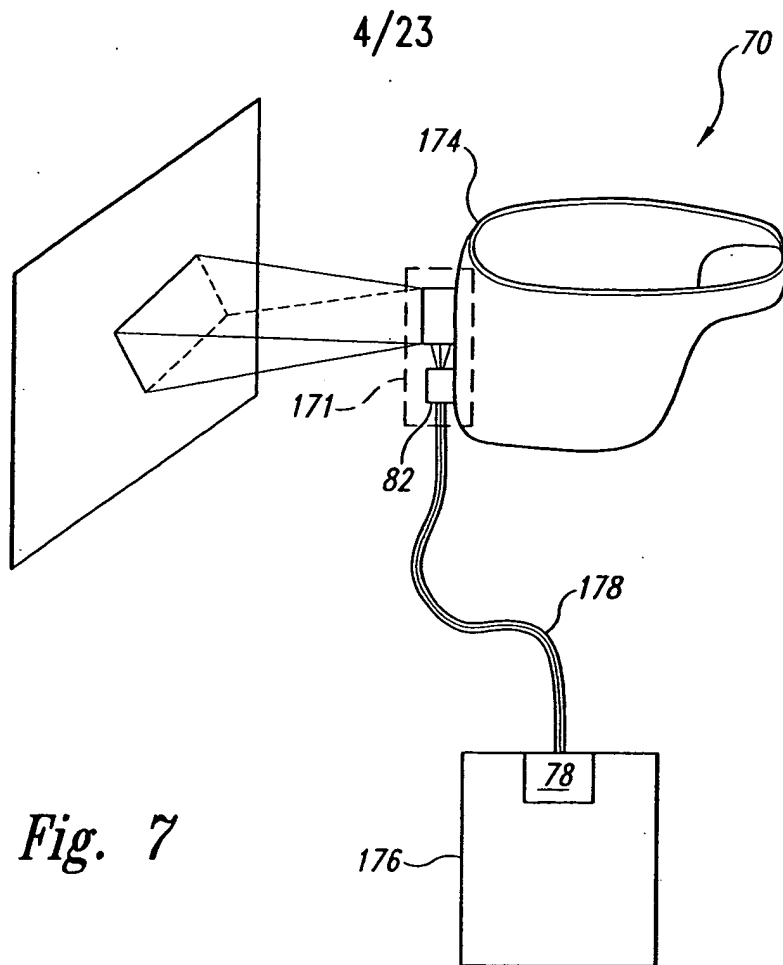
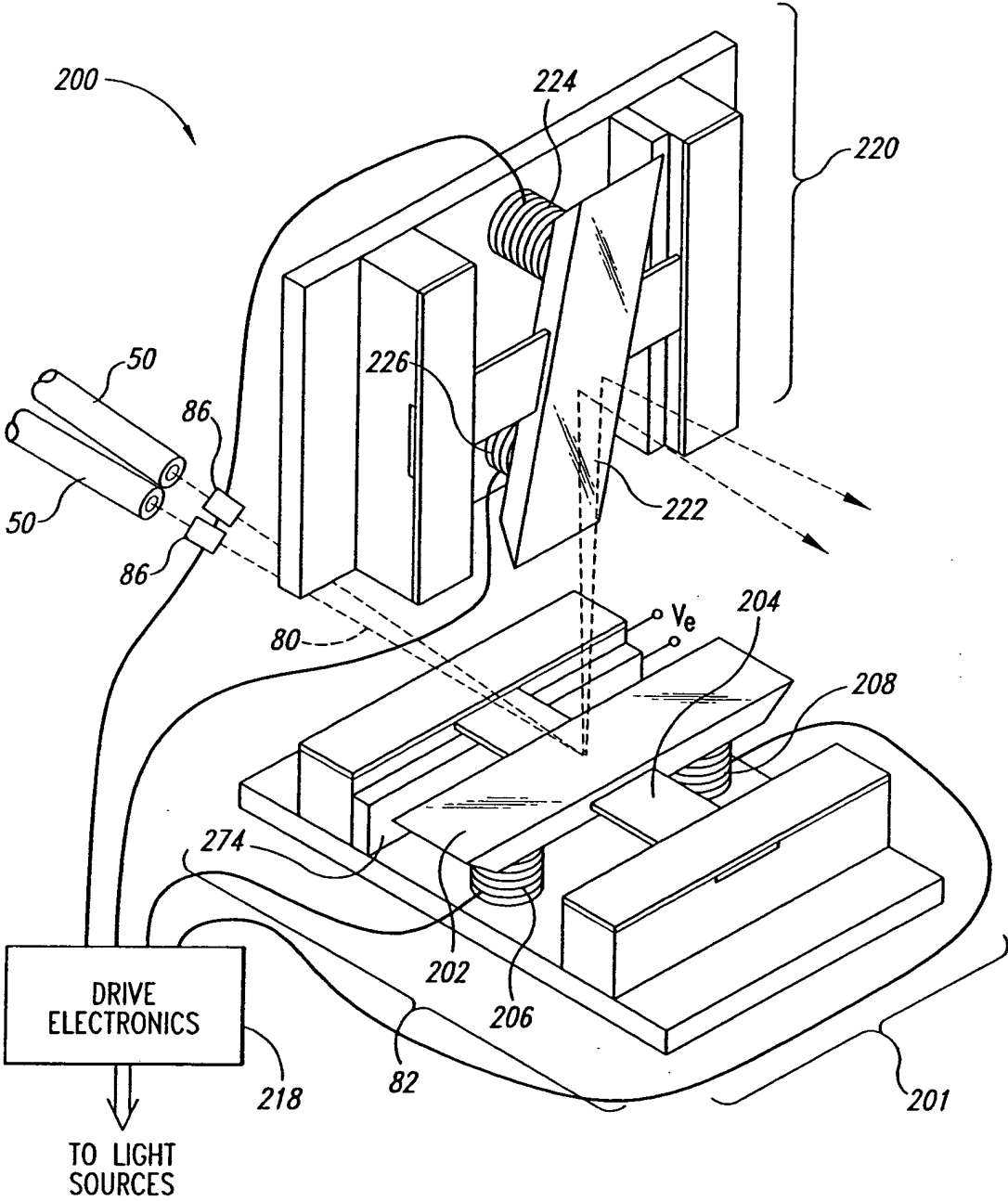


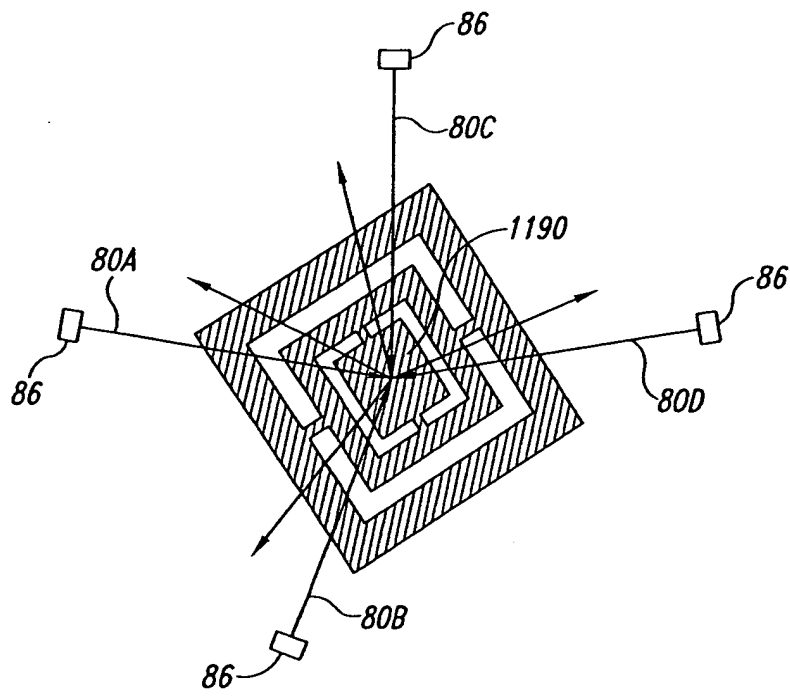
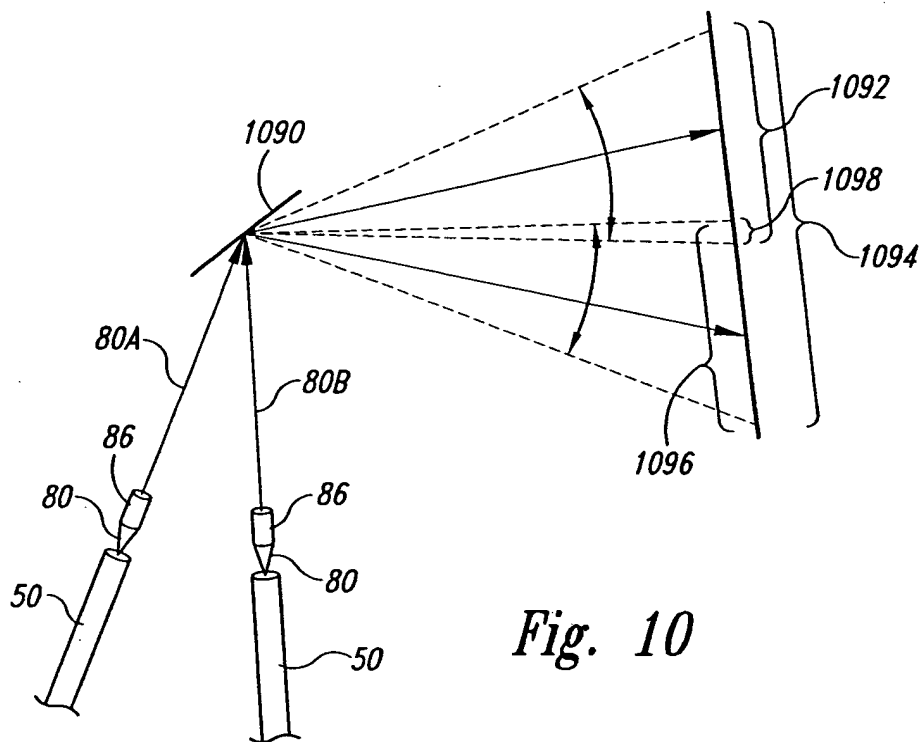
Fig. 6





*Fig. 9*

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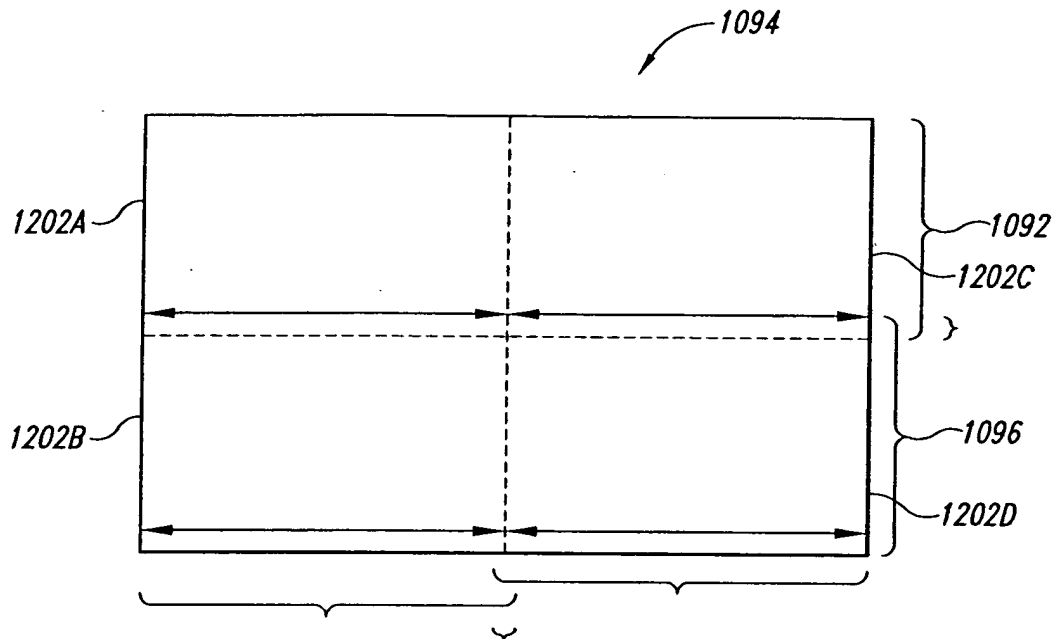


Fig. 12

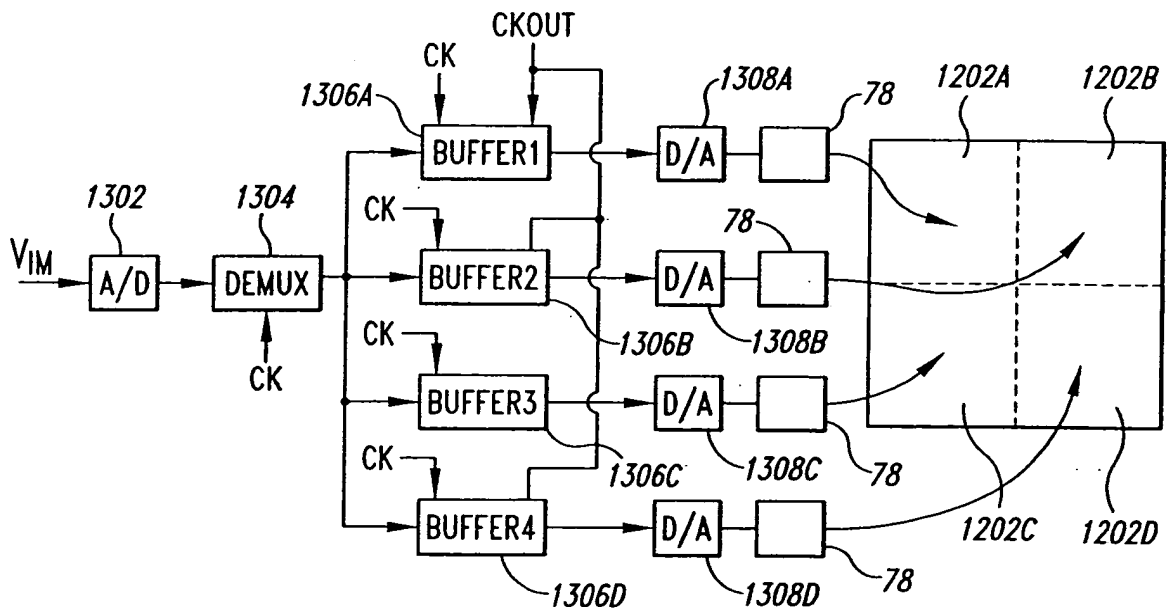
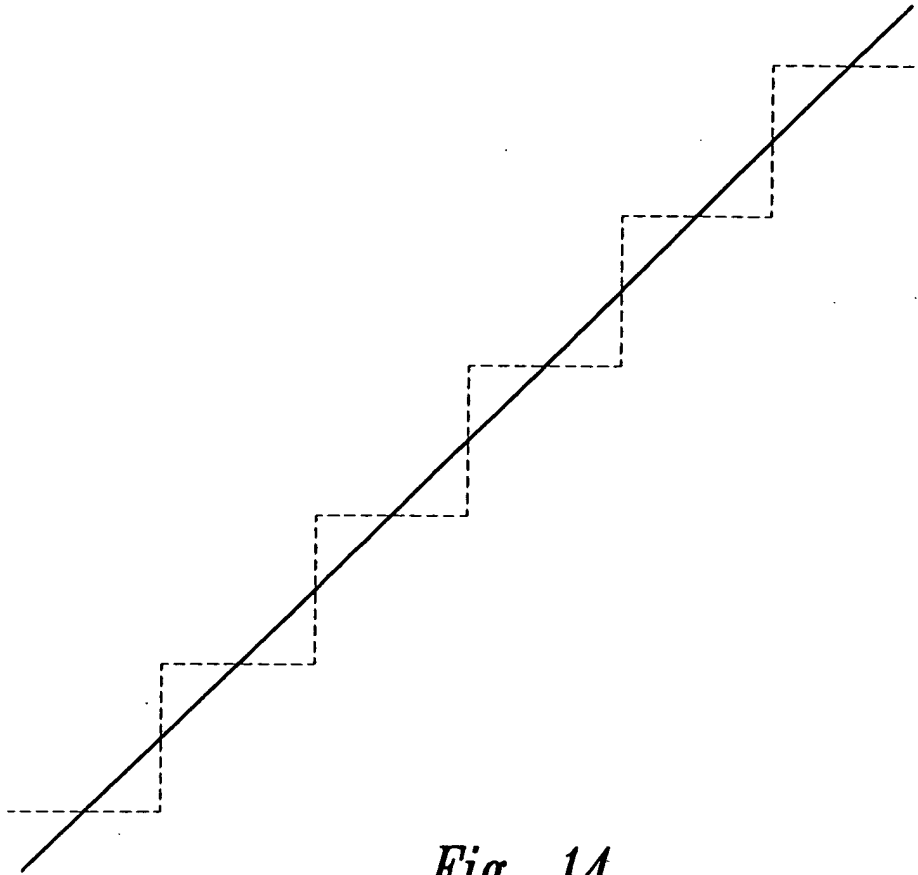
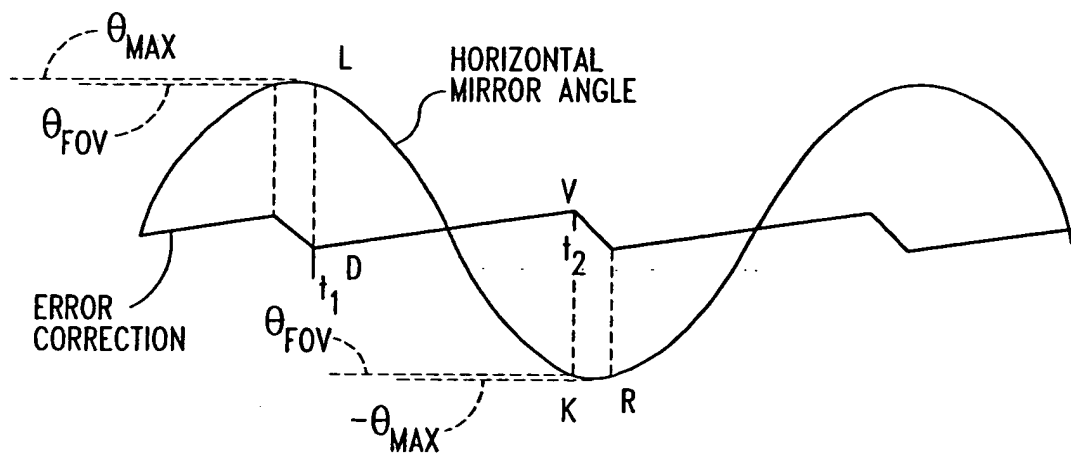


Fig. 13

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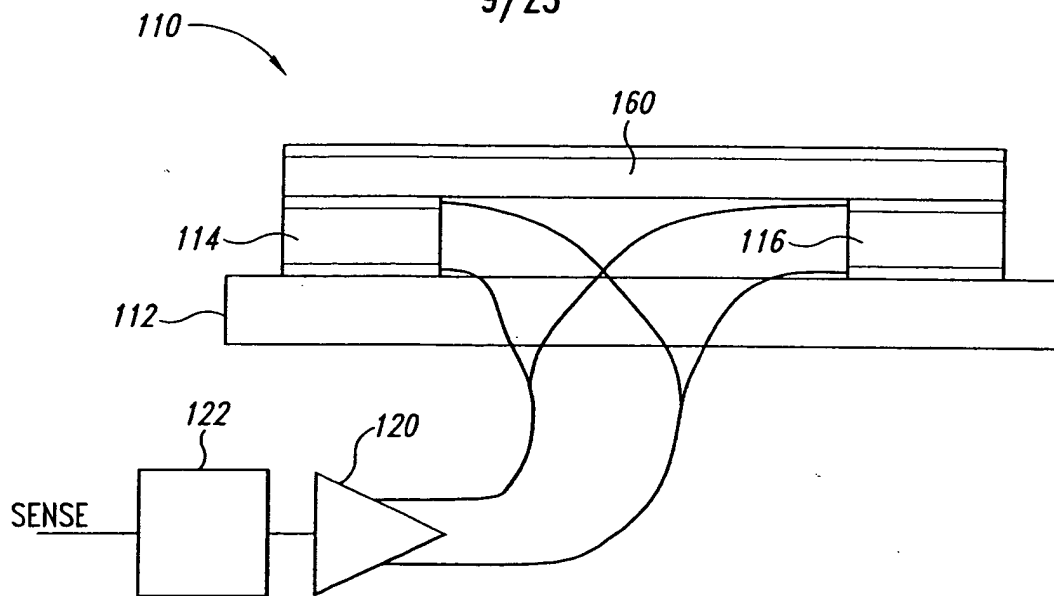
*Fig. 14*



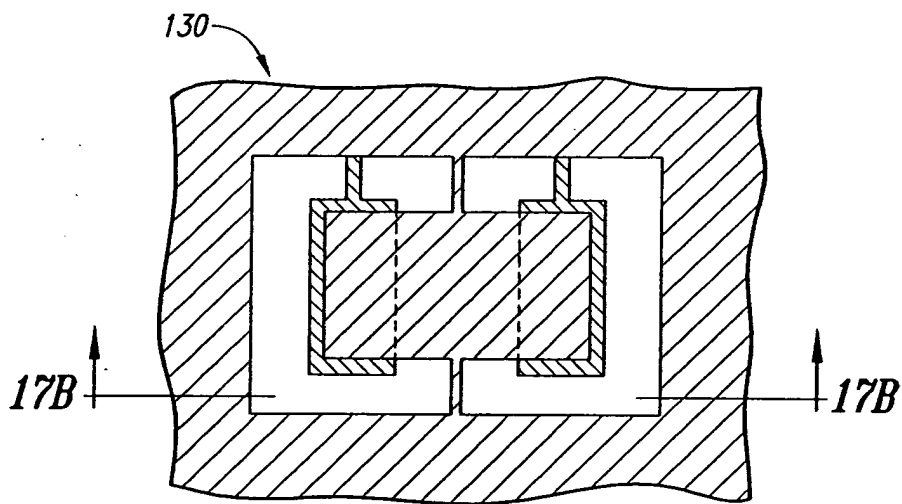
*Fig. 15*



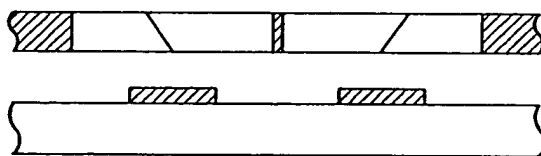
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*Fig. 16*

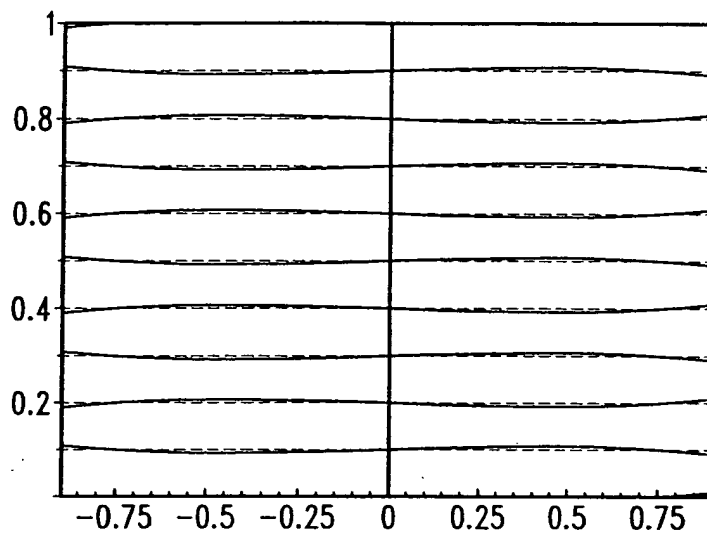


*Fig. 17A*

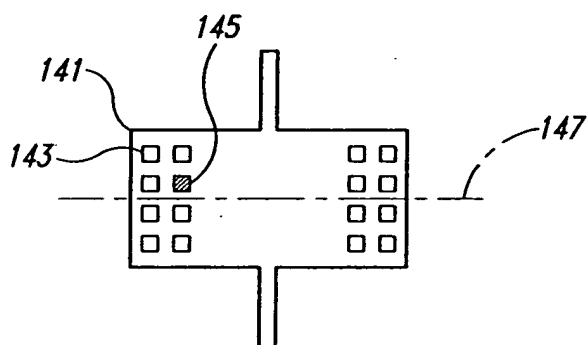


*Fig. 17B*

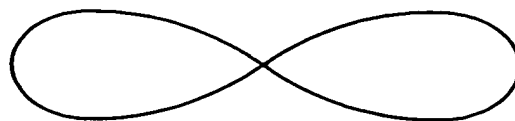
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*Fig. 18*



*Fig. 19*



*Fig. 20*

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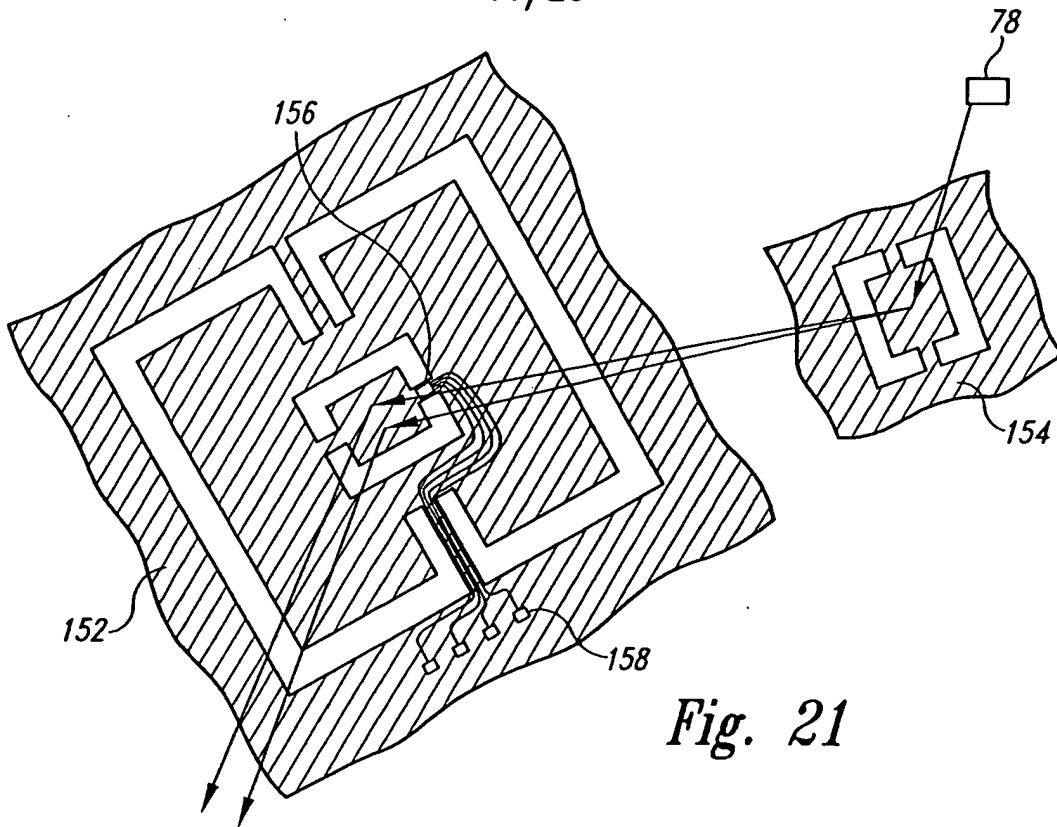


Fig. 21

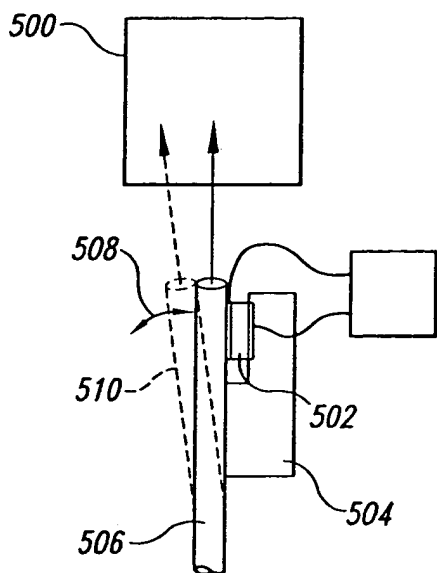


Fig. 22

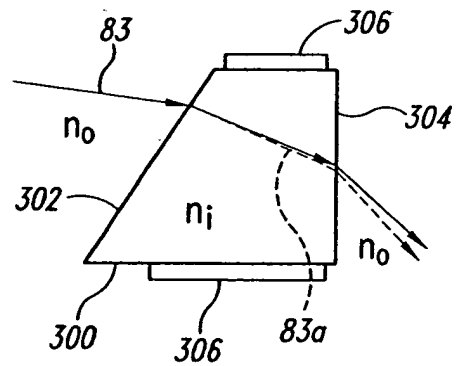
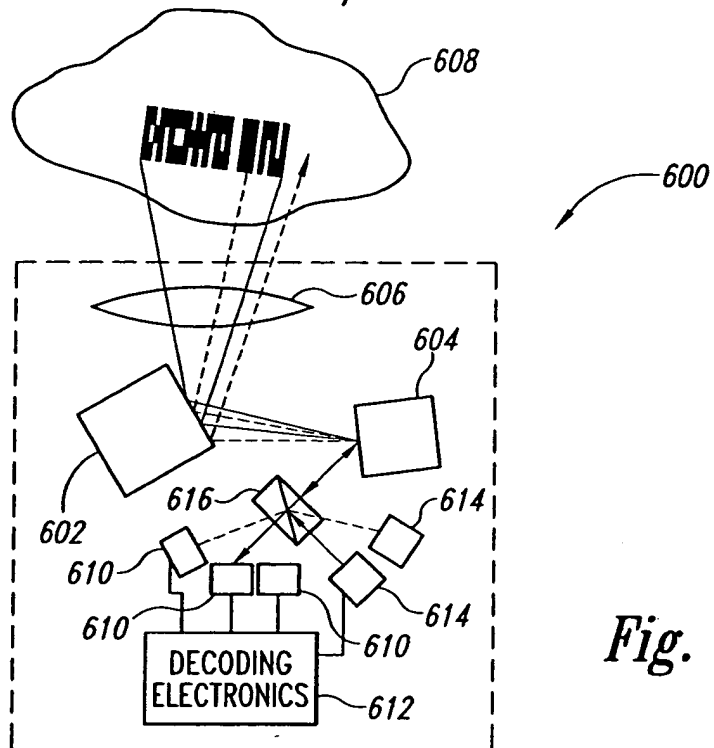
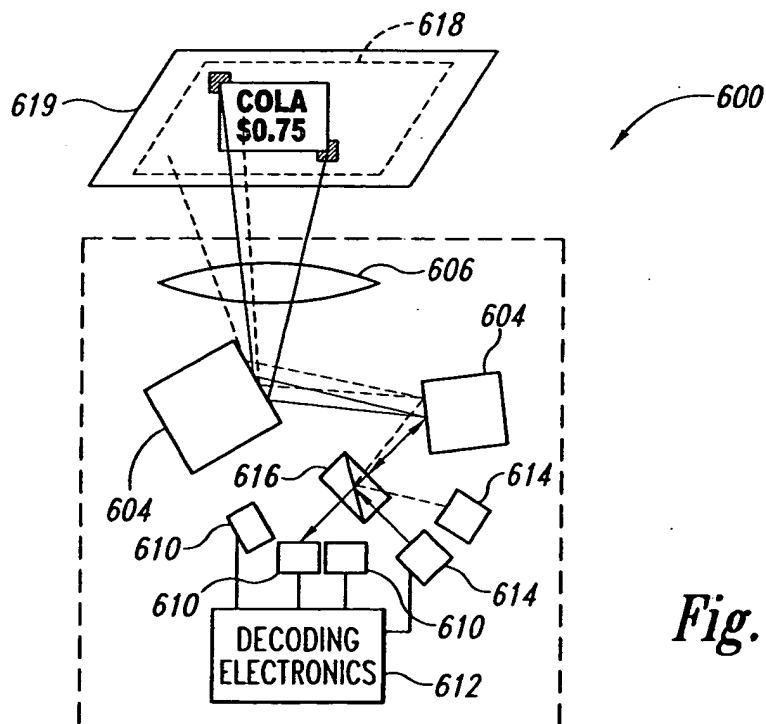


Fig. 23

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*Fig. 24*



*Fig. 25*

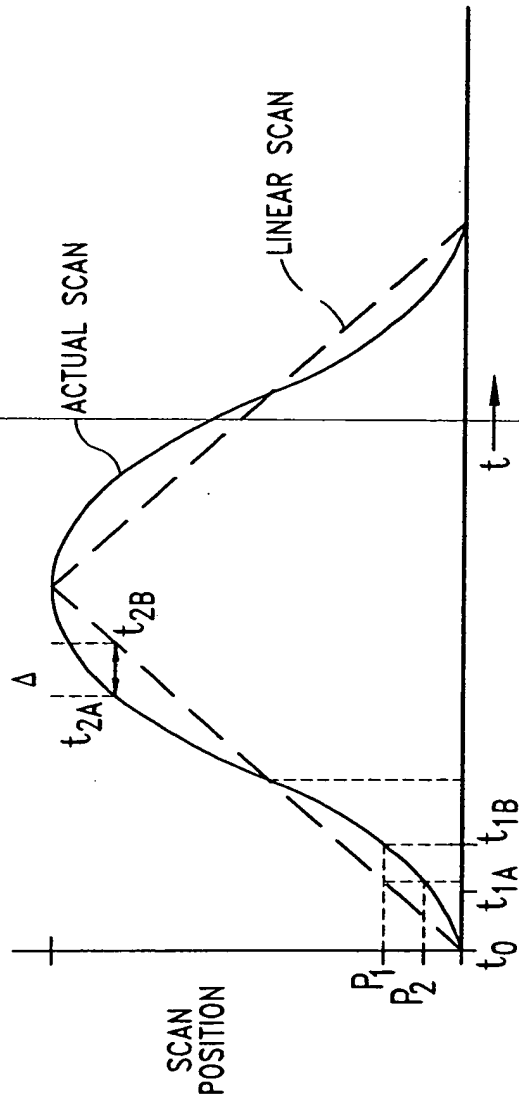


Fig. 26

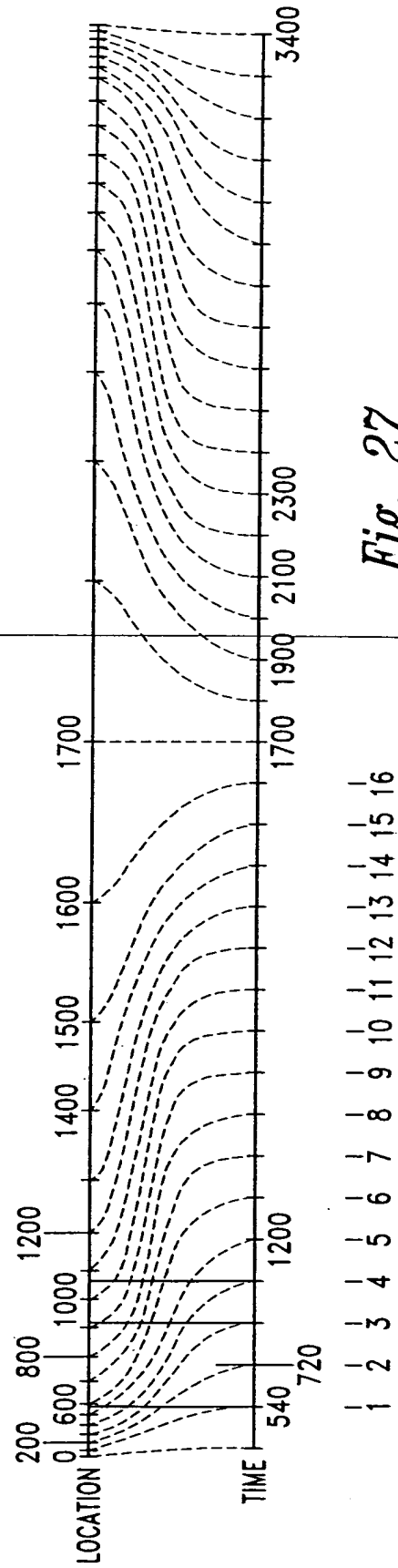


Fig. 27

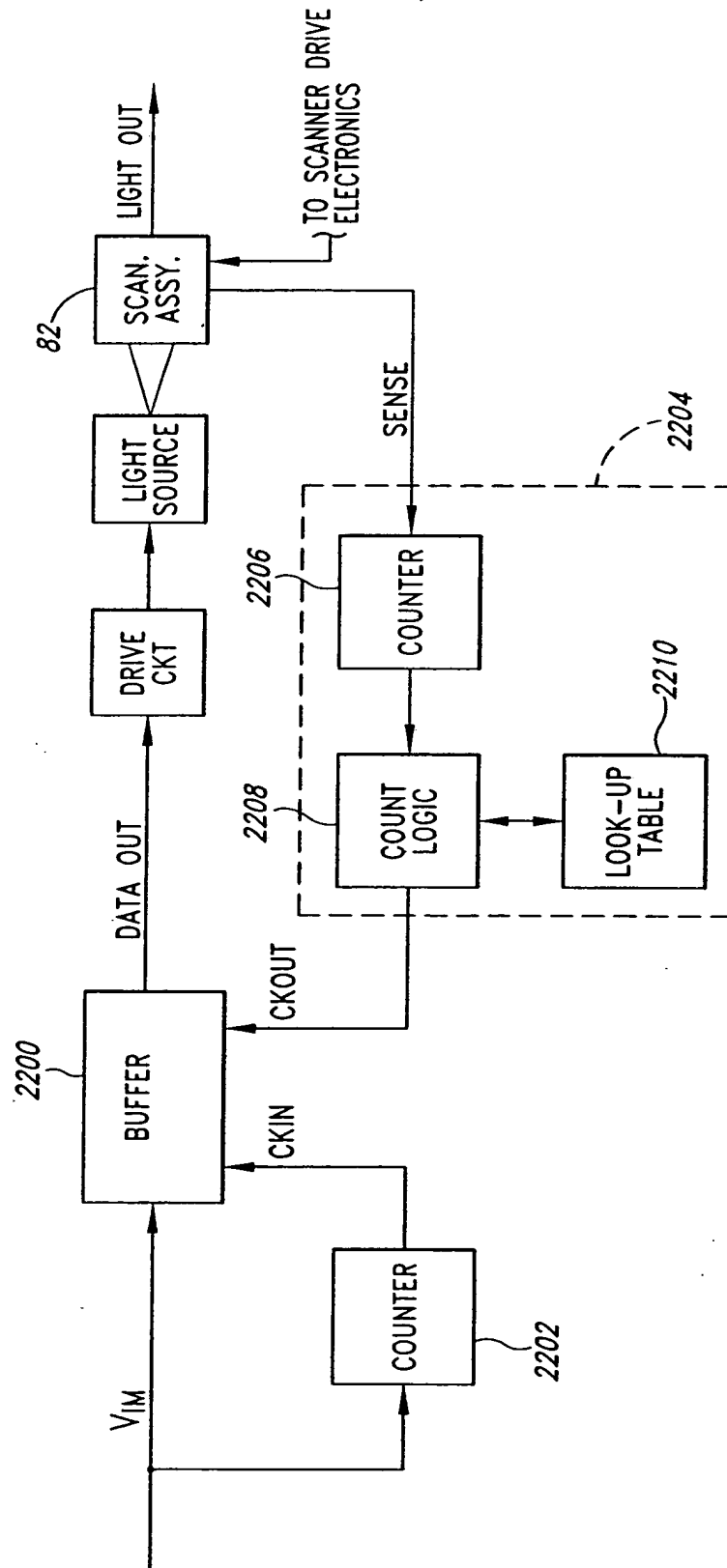


Fig. 28

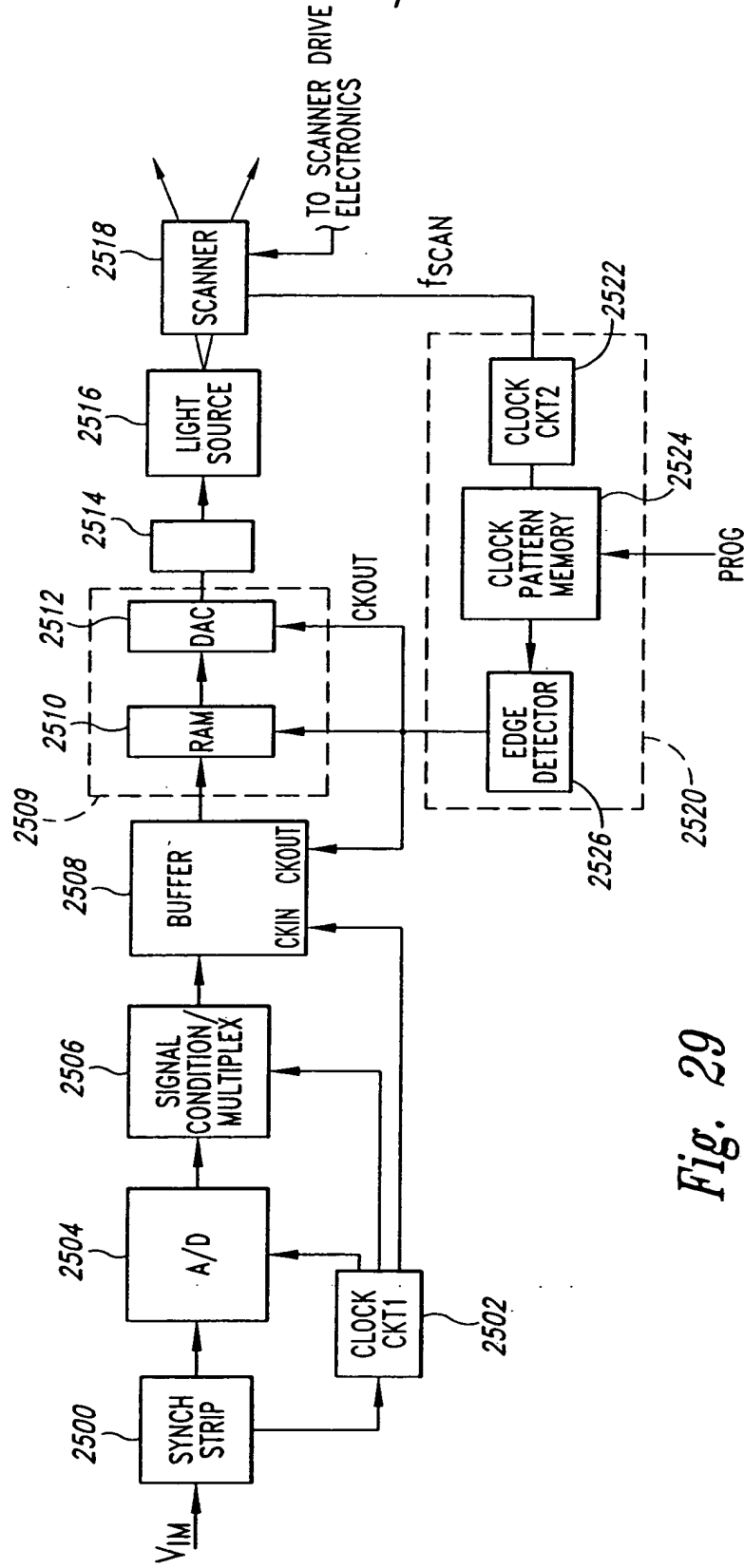


Fig. 29

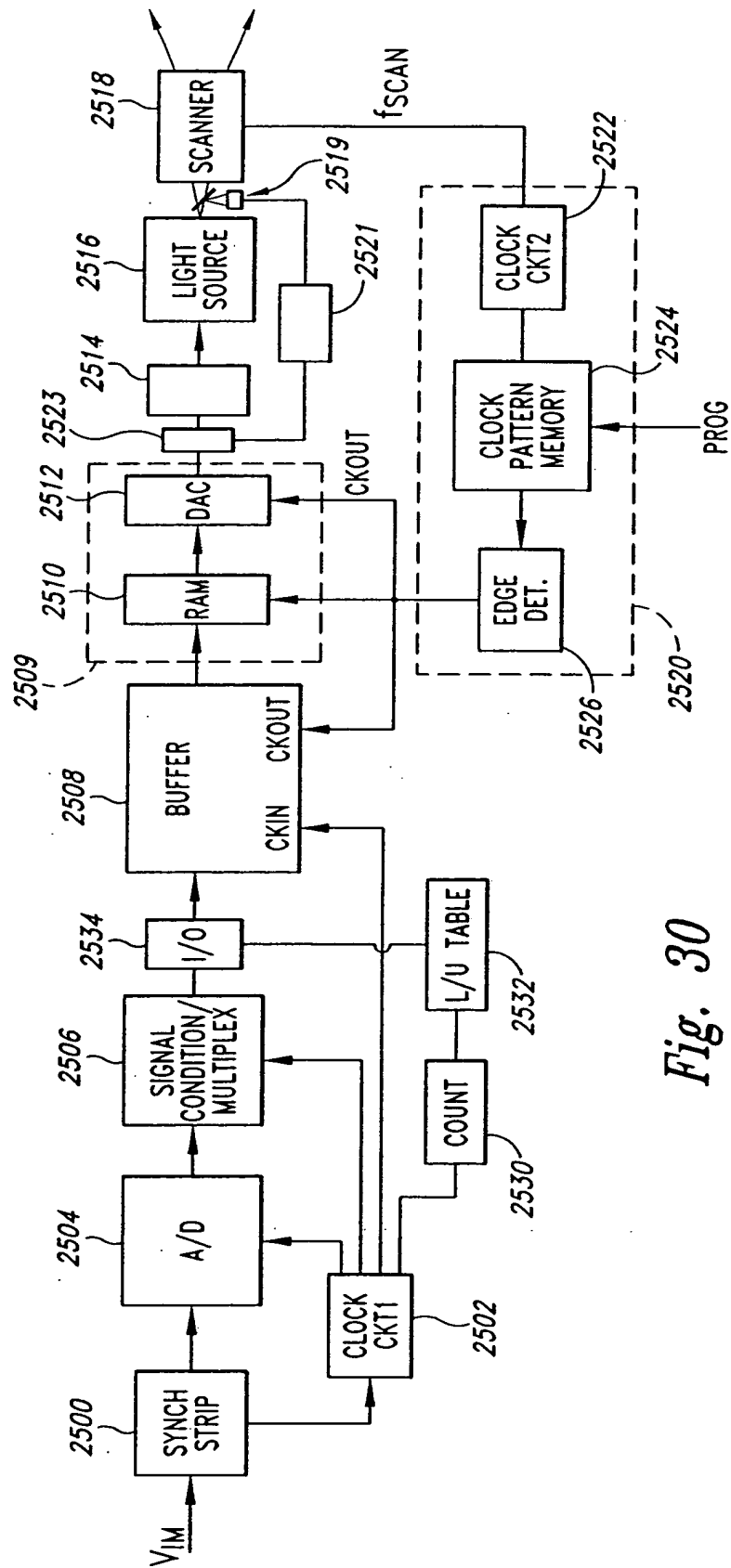


Fig. 30



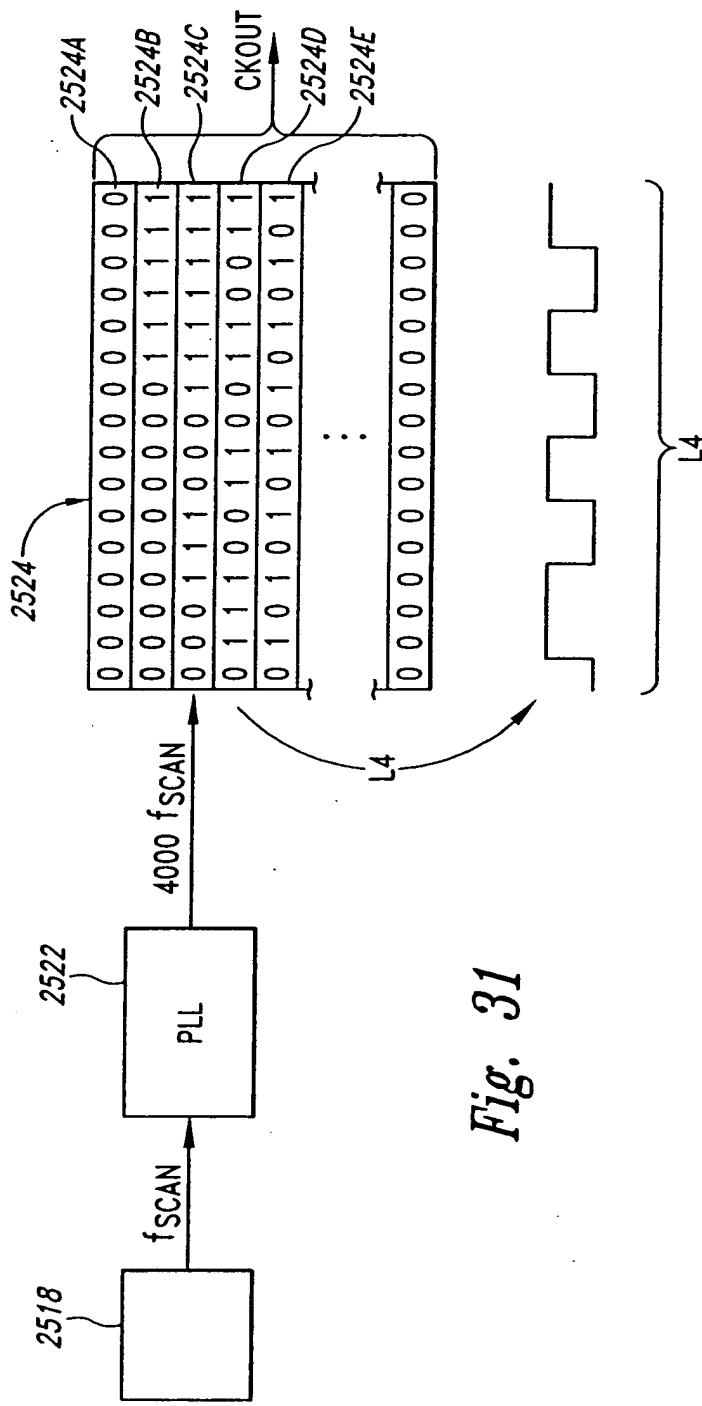
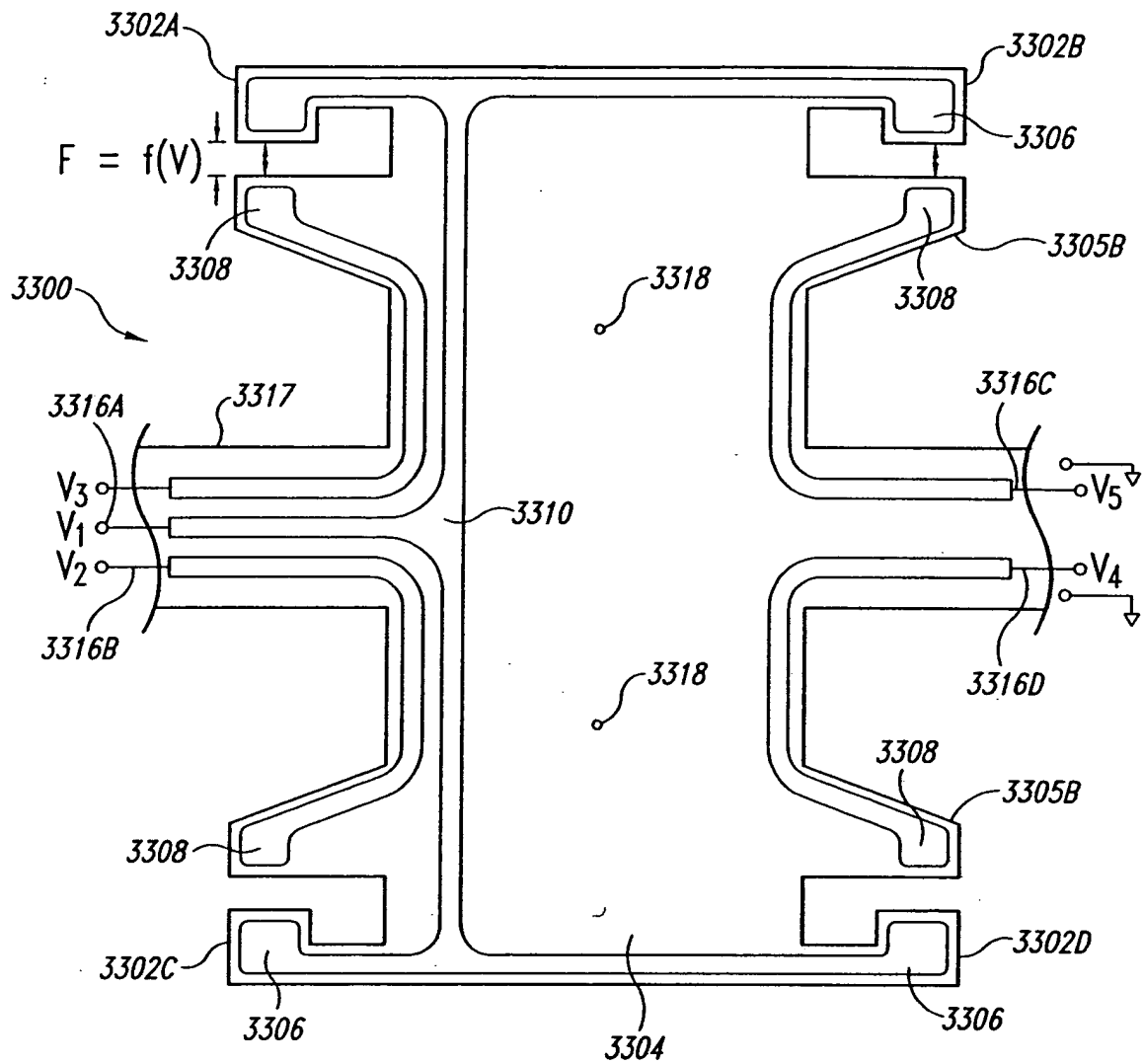


Fig. 31

Fig. 32 is a timing diagram and a data table. The timing diagram shows a square wave signal with a period labeled L4. The data table shows the data stored in registers 2524A through 2524E.

Register	2524A	2524B	2524C	2524D	2524E
Bit 7	0	0	0	0	0
Bit 6	0	0	0	0	0
Bit 5	0	0	0	0	0
Bit 4	0	0	0	0	0
Bit 3	0	0	0	0	0
Bit 2	0	0	0	0	0
Bit 1	0	0	0	0	0
Bit 0	0	0	0	0	0

Fig. 32



*Fig. 33*

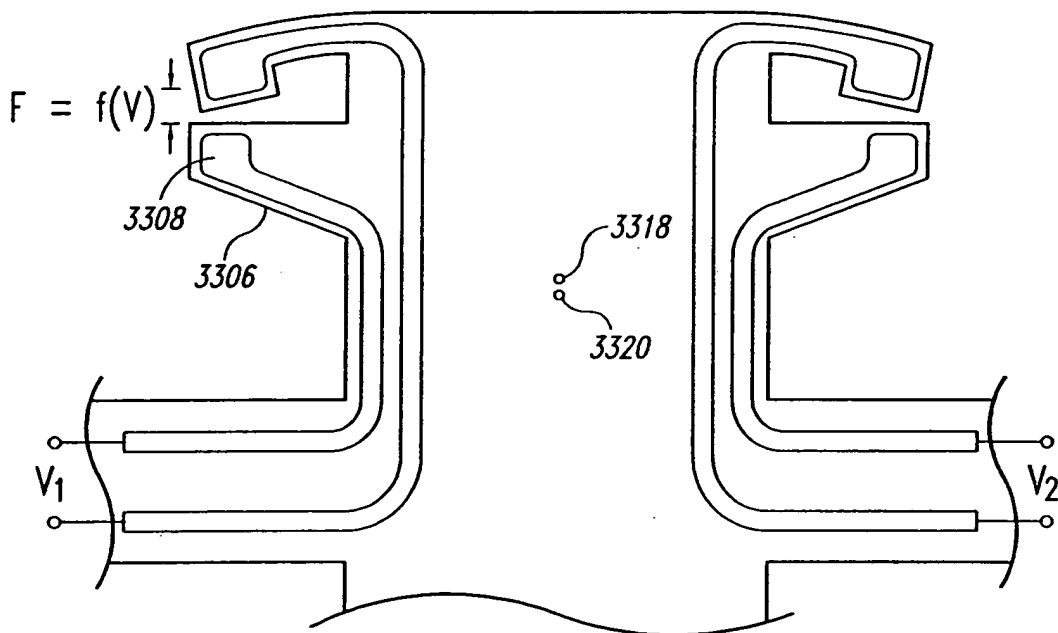


Fig. 34

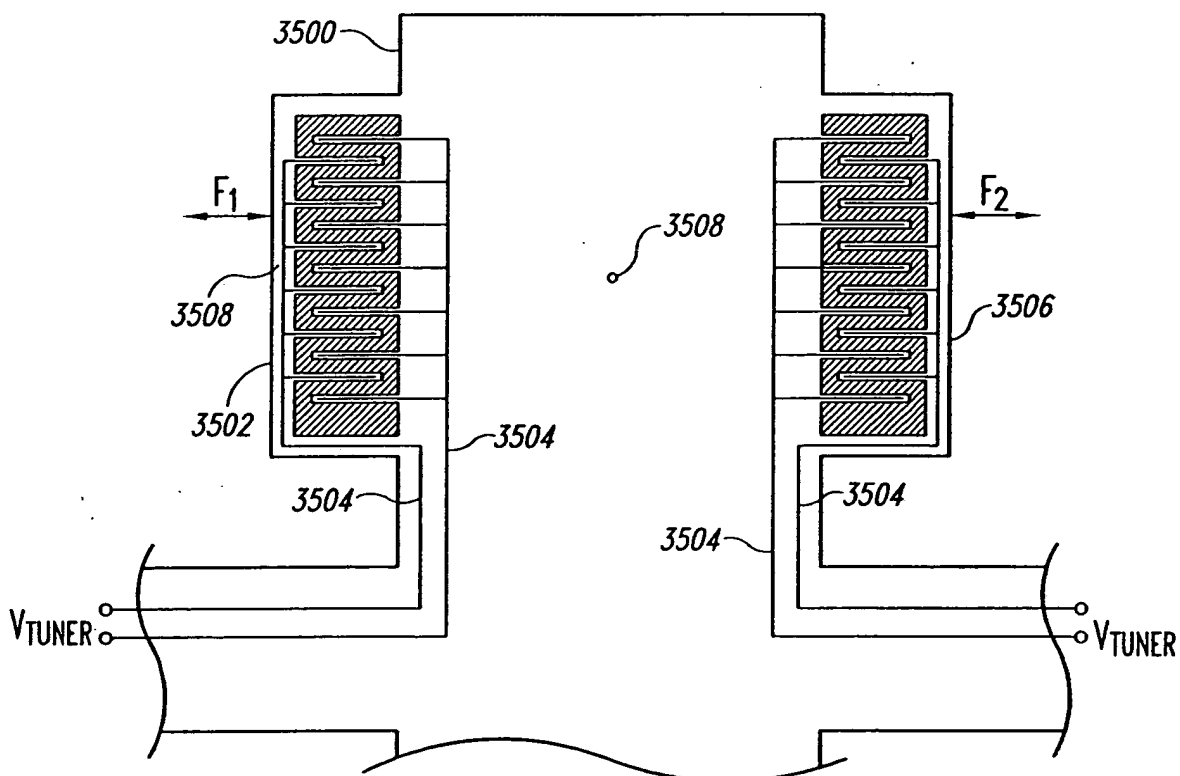


Fig. 35

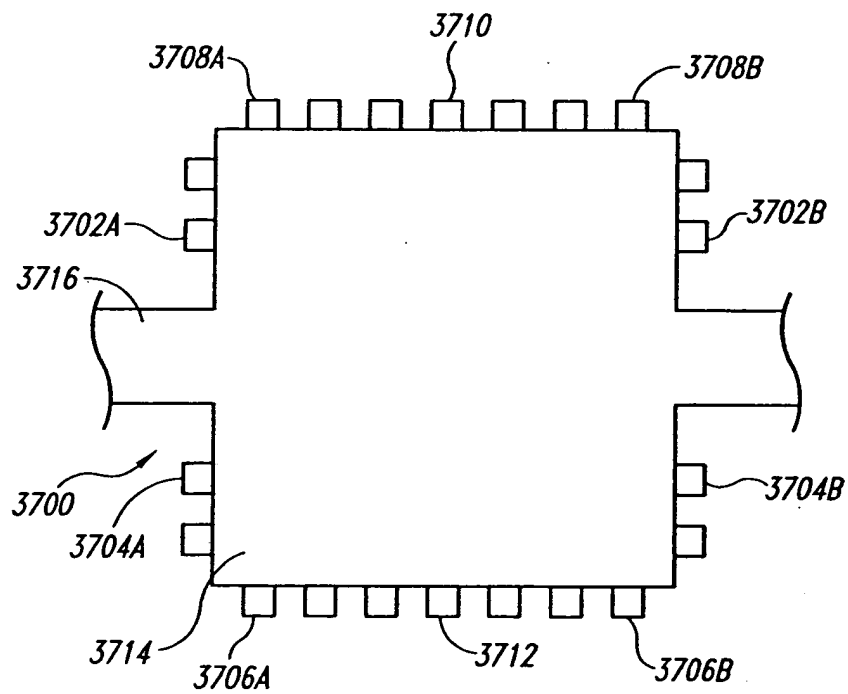
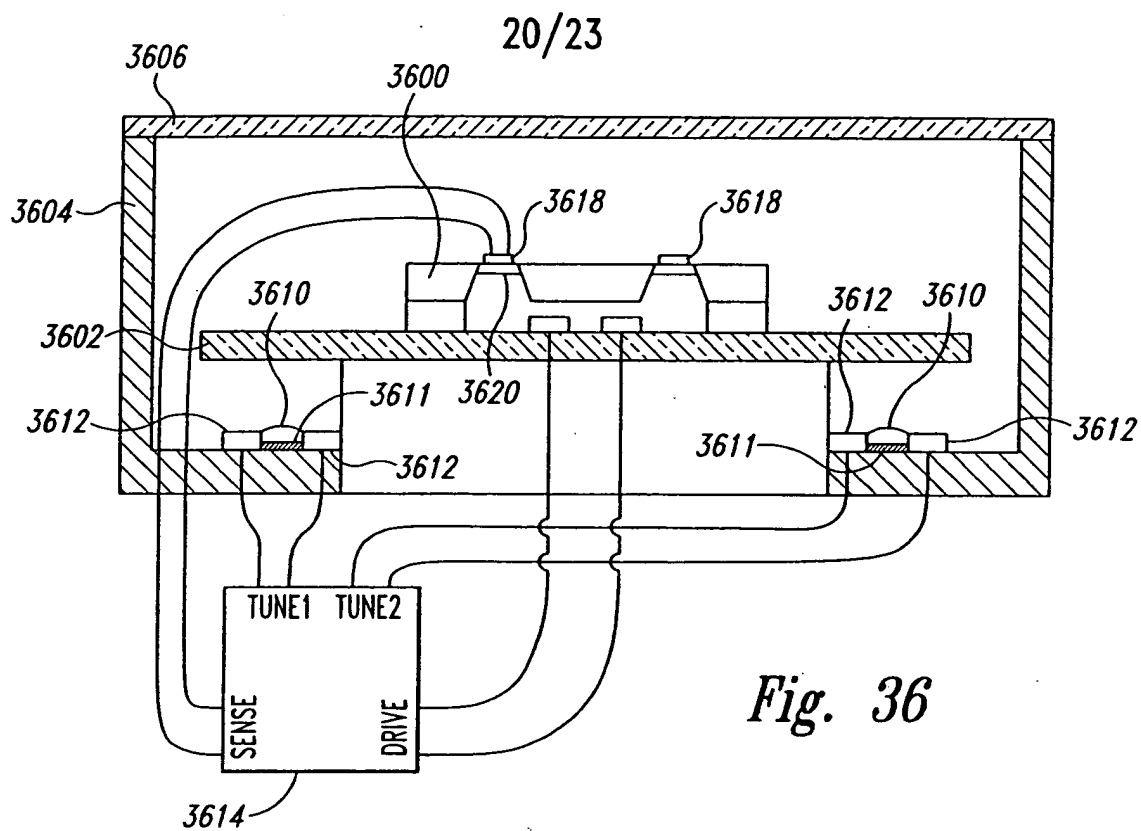
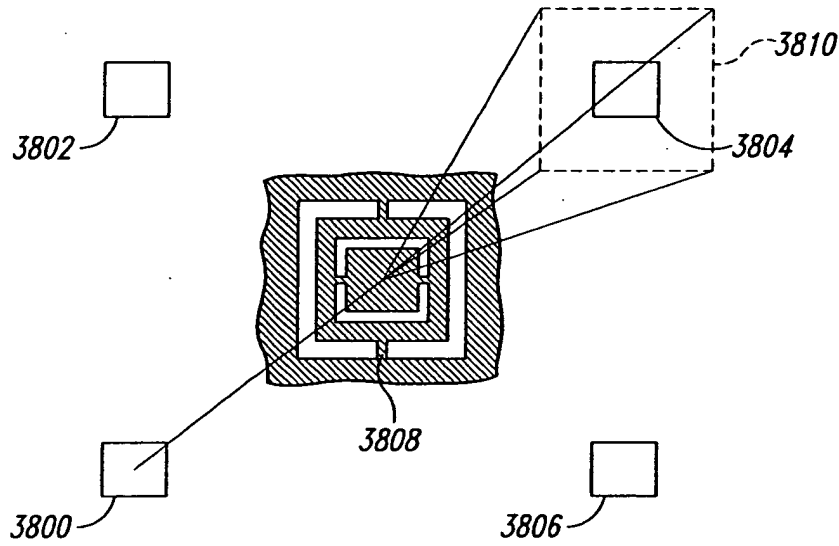
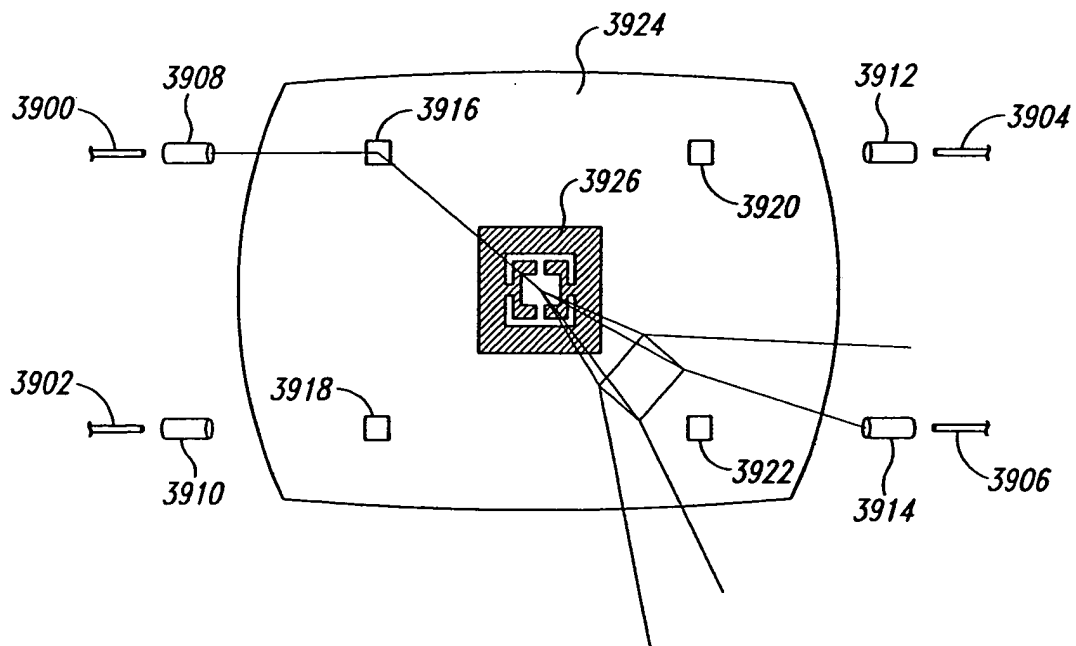


Fig. 37

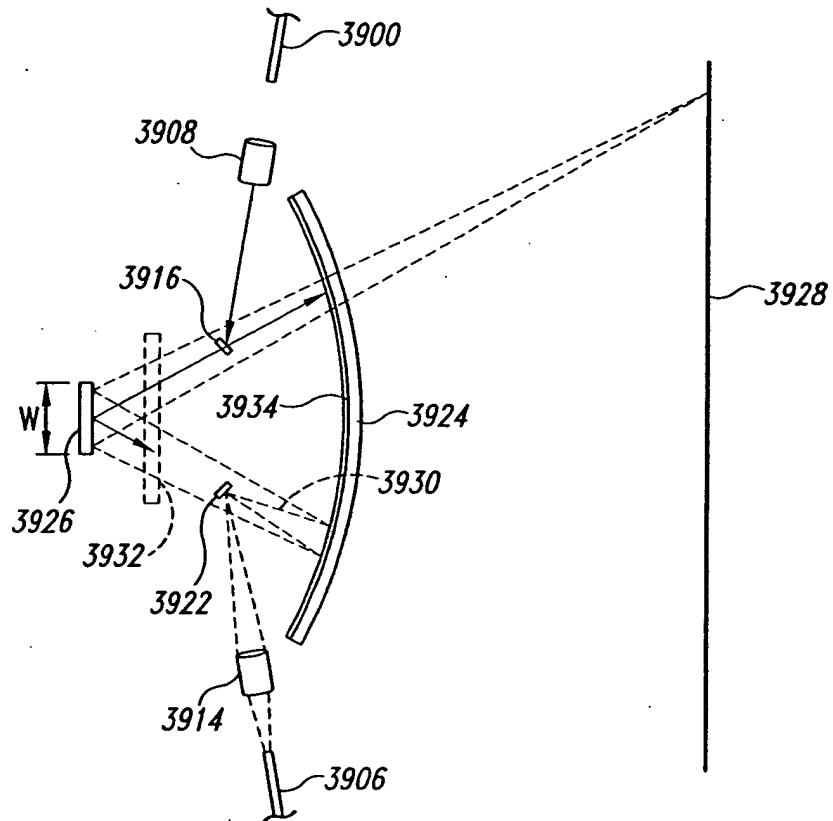
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*Fig. 38*



*Fig. 39*

*Fig. 40*

